Claims

[c1] What is claimed is:

1. A very long instruction word (VLIW) processor for executing a very long instruction word, the VLIW having a conditional execution head (CEX) and a plurality of operations, the VLIW processor comprising:

a plurality of functional units for executing operations in parallel;

an instruction register having a plurality of slots for holding the conditional execution head and the operations, the conditional execution head comprising a plurality of conditional indicators each specifying a condition under which a corresponding operation comprised in the VLIW is to be executed;

a plurality of switches each connected to a slot and a functional unit for controlling delivery of an operation from the slot to the functional unit for execution; and

a control circuit connected to the instruction register and each switch, the control circuit being capable of opening or closing the switch according to the condition specified in the corresponding conditional indicator;

wherein functional units which are connected to opened switches will receive operations from slots connected to the switches, functional units which are connected to closed switches will be prohibited from receiving operations, and operations which are received by functional units will be executed in parallel.

[c2] 2. The VLIW processor of claim 1 wherein each conditional indicator uniquely corresponds to only one operation comprised in the VLIW and each operation uniquely corresponds to only one conditional indicator comprised in the conditional execution head.

[c3] 3. The VLIW processor of claim 1 wherein the operation comprises an operational code specifying the operation to be executed by the functional unit.

[c4] 4. The VLIW processor of claim 1 further comprises a condition flag indicating the results of a comparison operation.

[c5] 5. The VLIW processor of claim 4 wherein the conditional indicator is a single bit.

[c6] 6. The VLIW processor of claim 5 wherein the condition to execute the operation is met when the conditional indicator and the condition flag are set to the same value.

[c7] 7. A very long instruction word (VLIW) processor having a plurality of functional units for executing a very long instruction word, the VLIW comprising a conditional execution head (CEX) and a plurality of operations, the maximum number of operations to be executed being equal to the number of functional units, the VLIW processor comprising:
an instruction register having a plurality of slots for holding the conditional execution head and the operations, the conditional execution head comprising a plurality of conditional indicators, the number of conditional indicators being equal to the number of operations comprised in the VLIW and each conditional indicator uniquely corresponding to only one operation, each conditional indicator indicating a condition under which the corresponding operation is to be executed;
a plurality of switches for controlling the delivery of the operation from the instruction register to the functional unit, each switch connecting only one slot and only one functional unit in a one-to-one correspondence; and
a control circuit connected to the instruction register and the switch, the control circuit capable of opening the switch when the condition indicating the corresponding operation is to be executed is met and for closing the switch when the condition indicating the corresponding operation is to be executed is not met.

[c8] 8. The VLIW processor of claim 7 wherein the operation comprises an operational code specifying the operation to be executed by the functional unit.

[c9] 9. The VLIW processor of claim 7 further comprises a condition flag indicating the results of a comparison operation.

[c10] 10. The VLIW processor of claim 9 wherein the condition to execute the operation is met when the conditional indicator and the condition flag are set to the same value.

[c11] 11. A method of program execution by a very long instruction word (VLIW) processor, the VLIW comprising a conditional execution head (CEX) and a plurality of operations, the conditional head comprising a plurality of conditional indicators, each conditional indicator corresponding to a predetermined operation and for specifying a condition when the operation is to be executed, the VLIW processor comprising an instruction register having a plurality of slots for holding the conditional execution head and the operations, a plurality of functional units for executing operations in parallel, and a plurality of switches, each switch in a one-to-one correspondence with and connected between only one slot and only one functional unit, the switch for controlling delivery of the operation to the functional unit, the method comprising:
opening the switch when the condition specified by the conditional indicator is met and closing the switch when the condition specified by the conditional indicator is not met.

[c12] 12. The method of claim 11 wherein the VLIW processor further comprises a condition flag indicating the results of a comparison operation.

[c13] 13. The method of claim 12 wherein the condition to execute the operation is met when the conditional indicator and the condition flag are set to the same value.